L Number	Hits	Search Text	DB	Time stamp
1	52	(CDFG or (control adj2 data adj2 flow adj2 graph)) and 716/$.ccls.	USPAT	2004/11/14 07:54
5	552	high near2 level near2 synthesis	USPAT	2004/11/14 07:58
6	45	(high near2 level near2 synthesis) and ((CDFG or (control adj2 data adj2 flow adj2 graph)))	USPAT	2004/11/14 07:58
7	33	((high near2 level near2 synthesis) and ((CDFG or (control adj2 data adj2 flow adj2 graph)))) and ((CDFG or (control adj2 data adj2 flow adj2 graph)) and schedul$4 and synthesis and behavior)	USPAT	2004/11/14 07:58
10	20	((((high near2 level near2 synthesis) and ((CDFG or (control adj2 data adj2 flow adj2 graph)))) and ((CDFG or (control adj2 data adj2 flow adj2 graph)) and schedul$4 and synthesis and behavior)) and input and output) and constraint	USPAT	2004/11/14 08:00
11	29	((((high near2 level near2 synthesis) and ((CDFG or (control adj2 data adj2 flow adj2 graph)))) and ((CDFG or (control adj2 data adj2 flow adj2 graph)) and schedul$4 and synthesis and behavior)) and input and output) and constraint	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/11/14 08:00
8	33	(((high near2 level near2 synthesis) and ((CDFG or (control adj2 data adj2 flow adj2 graph)))) and ((CDFG or (control adj2 data adj2 flow adj2 graph)) and schedul$4 and synthesis and behavior)) and input and output	USPAT	2004/11/14 08:15
4	67	(CDFG or (control adj2 data adj2 flow adj2 graph))	USPAT	2004/11/14 08:15
3	38	(CDFG or (control adj2 data adj2 flow adj2 graph)) and schedul$4 and synthesis and behavior	USPAT	2004/11/14 08:16
2	26	(CDFG or (control adj2 data adj2 flow adj2 graph)) same schedul$4	USPAT	2004/11/14 08:29
12	23	(CDFG or (control adj2 data adj2 flow adj2 graph)) same schedul$4 and allocation	USPAT	2004/11/14 08:29
13	23	(CDFG or (control adj2 data adj2 flow adj2 graph)) same schedul$4 and allocation and generat$4	USPAT	2004/11/14 08:40
14	18	(CDFG or (control adj2 data adj2 flow adj2 graph)) same schedul$4 and allocation and (generat$4 same circuit)	USPAT	2004/11/14 09:00

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040148150 A1	20040729	42	Verification of scheduling in the presence of loops using uninterpreted symbolic simulation	703/14
2	US 20040083443 A1	20040429	45	High-level synthesis method	716/18
3	US 20030126580 A1	20030703	14	High level synthesis method and apparatus	716/18
4	US 20030028854 A1	20030206	35	High level synthesis method, thread generated using the same, and method for generating circuit including such threads	716/18
5	US 20020188923 A1	20021212	26	High-level synthesis apparatus, high-level synthesis method, method for producing logic circuit using the high-level synthesis method, and recording medium	716/18
6	US 20020162097 A1	20021031	35	Compiling method, synthesizing system and recording medium	717/155
7	US 20020124012 A1	20020905	19	Compiler for multiple processor and distributed memory architectures	707/200
8	US 20020053069 A1	20020502	28	High-level synthesis method, high-level synthesis apparatus, method for producing logic circuit using the high-level synthesis method for logic circuit design, and recording medium	716/18
9	US 20020026305 A1	20020228	13	Optimised production of hardware from source programs involving multiplications	704/1
10	US 20020004927 A1	20020110	26	Method for designing ingegrated circuit	716/2
11	US 20010016936 A1	20010823	44	High- level synthesis method and storage medium storing the same	716/18

	Document ID	Issue Date	Pages	Title	Current OR
12	US 20010011363 A1	20010802	25	Circuit synthesis method	716/18
13	US 6816828 B1	20041109	25	Logic simulation method in which simulation is dynamically switchable between models	703/15
14	US 6745160 B1	20040601	40	Verification of scheduling in the presence of loops using uninterpreted symbolic simulation	703/14
15	US 6704914 B2	20040309	33	High level synthesis method, thread generated using the same, and method for generating circuit including such threads	716/8
16	US 6687894 B2	20040203	27	High-level synthesis method, high-level synthesis apparatus, method for producing logic circuit using the high-level synthesis method for logic circuit design, and recording medium	716/18
17	US 6668337 B2	20031223	25	Method for designing integrated circuit based on the transaction analyzing model	714/6
18	US 6604232 B2	20030805	43	High-level synthesis method and storage medium storing the same	716/18
19	US 6532584 B1	20030311	23	Circuit synthesis method	716/18
20	US 6505340 B2	20030107	24	Circuit synthesis method	716/18
21	US 6493863 B1	20021210	44	Method of designing semiconductor integrated circuit	716/18
22	US 6449763 B1	20020910	19	High-level synthesis apparatus, high level synthesis method, and recording medium carrying a program for implementing the same	716/18

	Document ID	Issue Date	Pages	Title	Current OR
23	US 6438739 B1	20020820	17	High-level synthesis device high level synthesis method and recording medium with high level synthesis program	716/18
24	US 6363506 B1	20020326	15	Method for self-testing integrated circuits	714/733
25	US 6360355 B1	20020319	36	Hardware synthesis method, hardware synthesis device, and recording medium containing a hardware synthesis program recorded thereon	716/18
26	US 6195786 B1	20010227	19	Constrained register sharing technique for low power VLSI design	716/2
27	US 5764951 A	19980609	39	Methods for automatically pipelining loops	716/1
28	US 5706205 A	19980106	19	Apparatus and method for high-level synthesis of a logic circuit	716/18
29	US 5550749 A	19960827	13	High level circuit design synthesis using transformations	716/18
30	US 5513118 A	19960430	18	High level synthesis for partial scan testing	716/18
31	JP 2004164627 A	20040610	26	HIGH LEVEL SYNTHESIS METHOD	
32	JP 2003030261 A	20030131	19	HIGHER ORDER SYNTHESIS METHOD, THREAD GENERATED BY USING THE HIGHER ORDER SYNTHESIS METHOD AND METHOD FOR GENERATING CIRCUIT	
33	US 20040083443 A	20040602	45	High level synthesis method for large scale integrated circuit design, involves generating allocation information based on resource-level layout information and circuit information indicating resource relationship	